(12) UK Patent Application (19) GB (11) 2 345 369 (13) A

(43) Date of A Publication 05.07.2000

(21) Application No 0008387.3

(22) Date of Filing 17.01.1997

Date Lodged 05.04.2000

(30) Priority Data
(31) 08598766 (32) 09.02.1996 (33) US

(62) Divided from Application No 9700952.6 under Section 15(4) of the Patents Act 1977

(51) INT CL[7]
G06F 17/50 // H03K 19/177

(52) UK CL (Edition R)
G4H HU H13D

(56) Documents Cited
GB 2305528 A

(58) Field of Search
UK CL (Edition R) G4H HU
INT CL[7] G06F, H03K

(71) Applicant(s)
Hewlett-Packard Company
(Incorporated in USA - Delaware)
3000 Hanover Street, Palo Alto, California 94304,
United States of America

(72) Inventor(s)
Alireza S. Kaviani

(74) Agent and/or Address for Service
Carpmaels & Ransford
43 Bloomsbury Square, LONDON, WC1A 2RA,
United Kingdom

(54) Abstract Title
Implementing logic circuits

(57) A programmable monolithic integrated logic circuit includes look up table circuits and programmable logic array-like circuits. The integrated circuit can include a first number of the look up tables and a second number of the programmable logic array-like circuits and where the first and second numbers are related by a ratio of between 0.25:1 and 6:1, between 1:1 and 5:1, or about 4:1. The programmable logic array-like circuits can each include at least 10,000 or 50,000 equivalent two-input NAND gates and the look up tables and the programmable logic array-like circuits can each comprise static random access cells. A method of implementing a logic circuit includes reading a netlist that includes a plurality of subnets, determining the suitability of ones of the subnets to being implemented with look up tables and with programmable logic array-like circuits, and determining whether to implement each subnet with a look up table or a programmable logic array-like circuit based on results of the step of determining. Based on the steps of determining, the method implements a first subnet of the plurality of subnets with look up table circuits and a second subset of the plurality of subnets with programmable logic array-like circuits.

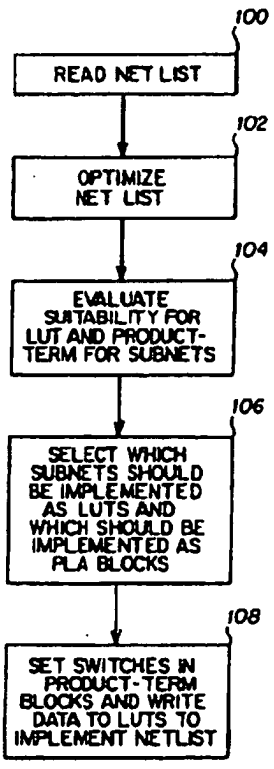

FIG. 6

GB 2 345 369 A

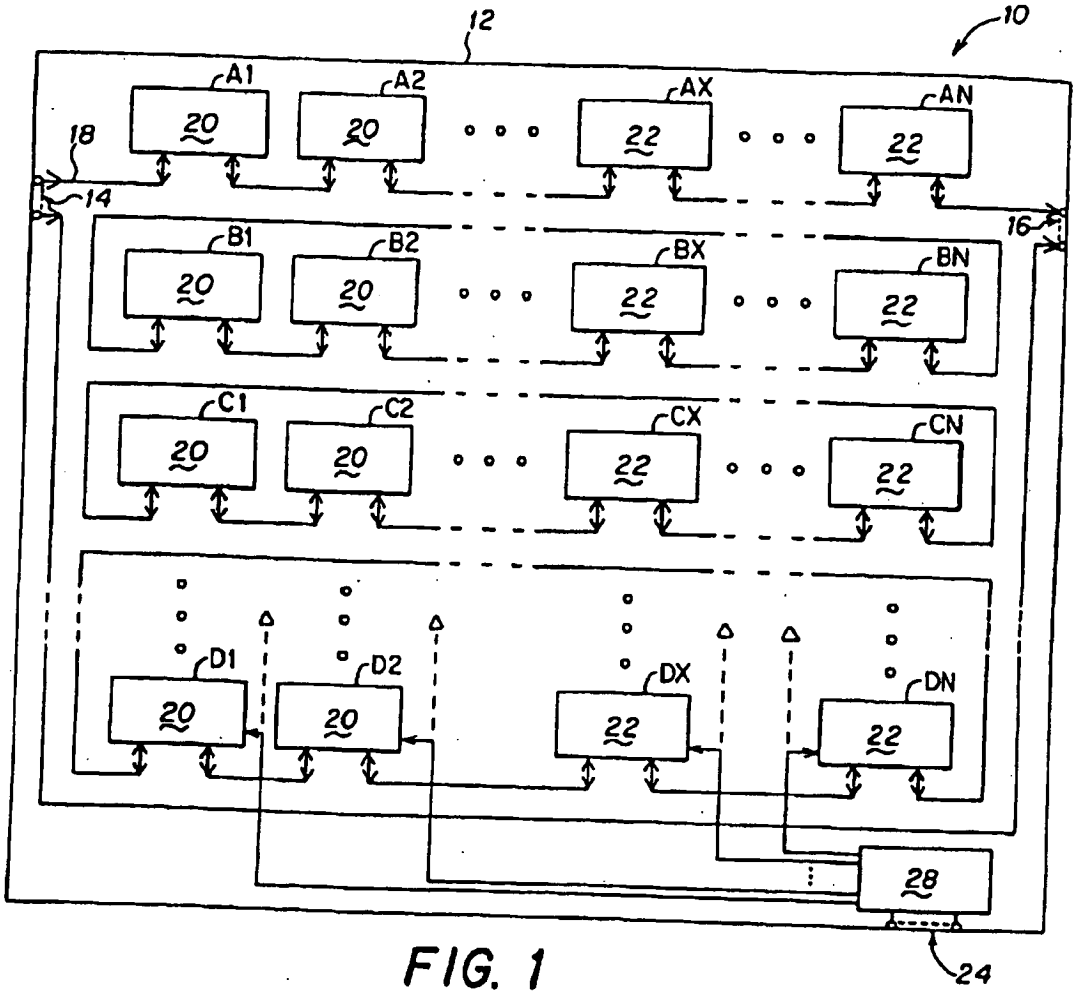
12
10
A1
A2
AX
AN
18
14
16
B1
B2
BX
BN
C1
C2
CX
CN
D1
D2
DX
DN
20
22
28
24

FIG. 1

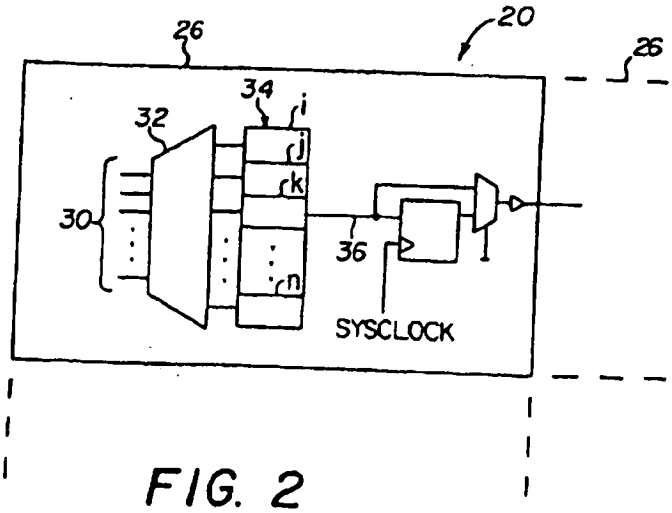
26
20
26
34
i
32
j
k
30
n
36
SYSCLOCK

FIG. 2

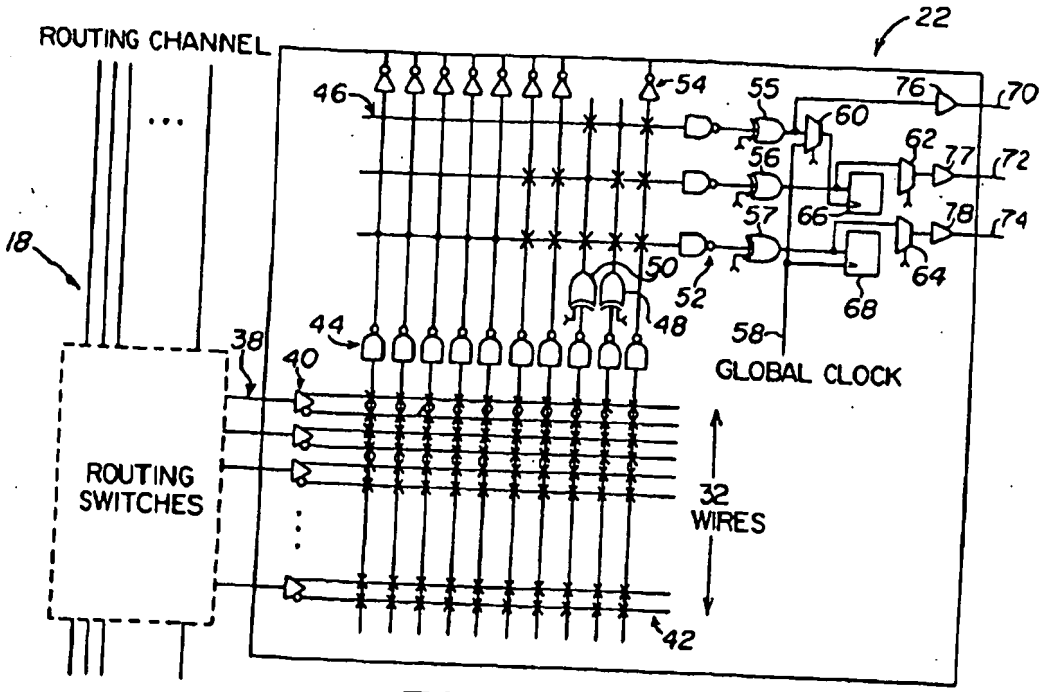

FIG. 3

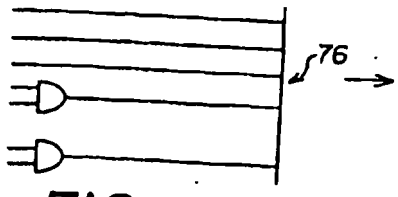

FIG. 4A

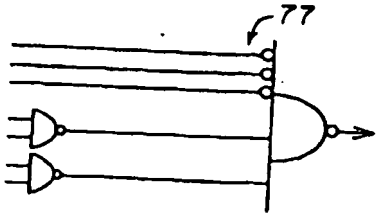

FIG. 4B

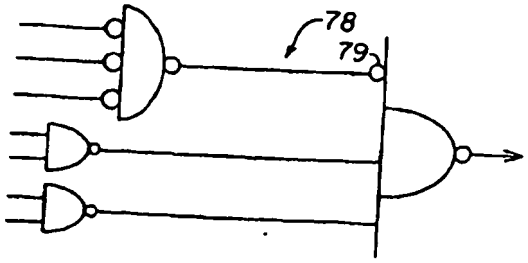

FIG. 4C

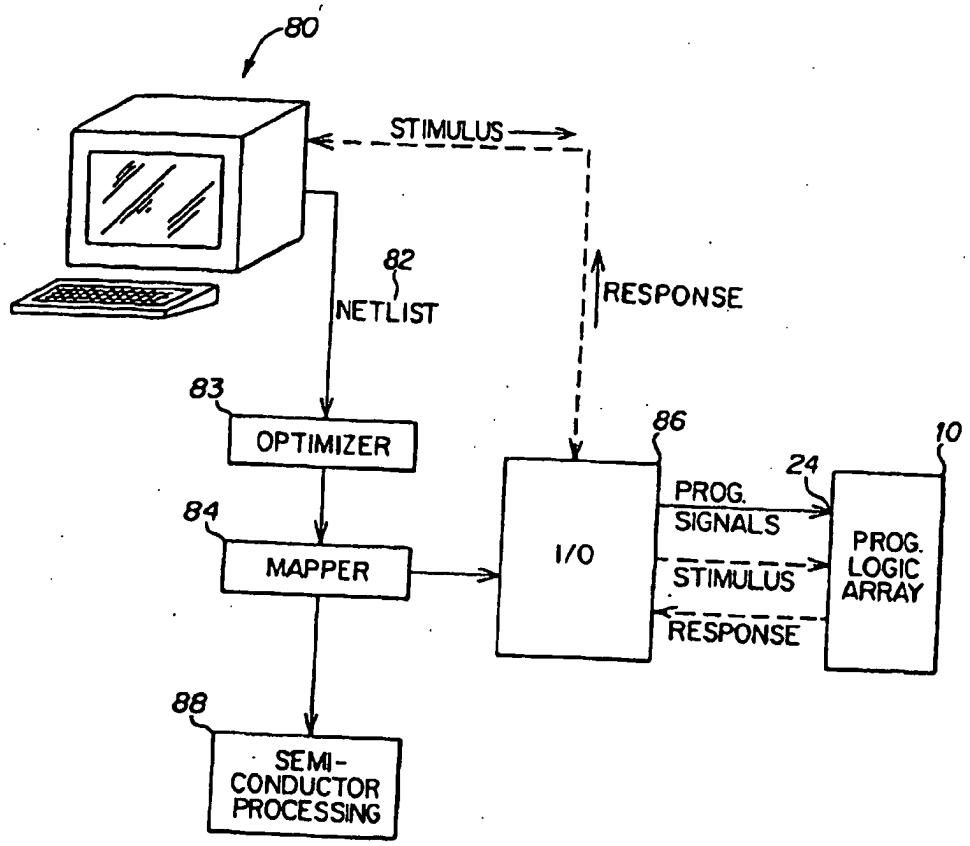
80
STIMULUS
82
NETLIST
RESPONSE
83
OPTIMIZER
86
10
24
84
MAPPER
I/O
PROG.
SIGNALS
PROG.
LOGIC
ARRAY
STIMULUS
RESPONSE
88
SEMI-
CONDUCTOR
PROCESSING

FIG. 5

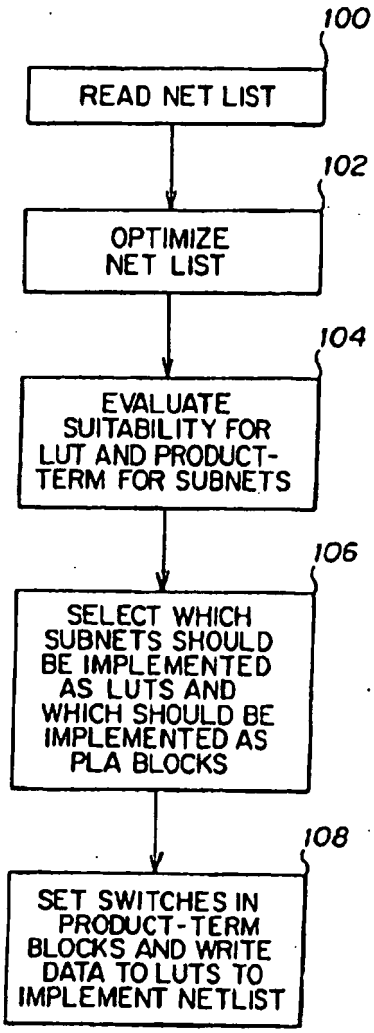
100
READ NET LIST
102
OPTIMIZE NET LIST
104
EVALUATE SUITABILITY FOR LUT AND PRODUCT-TERM FOR SUBNETS
106
SELECT WHICH SUBNETS SHOULD BE IMPLEMENTED AS LUTS AND WHICH SHOULD BE IMPLEMENTED AS PLA BLOCKS
108
SET SWITCHES IN PRODUCT-TERM BLOCKS AND WRITE DATA TO LUTS TO IMPLEMENT NETLIST

FIG. 6

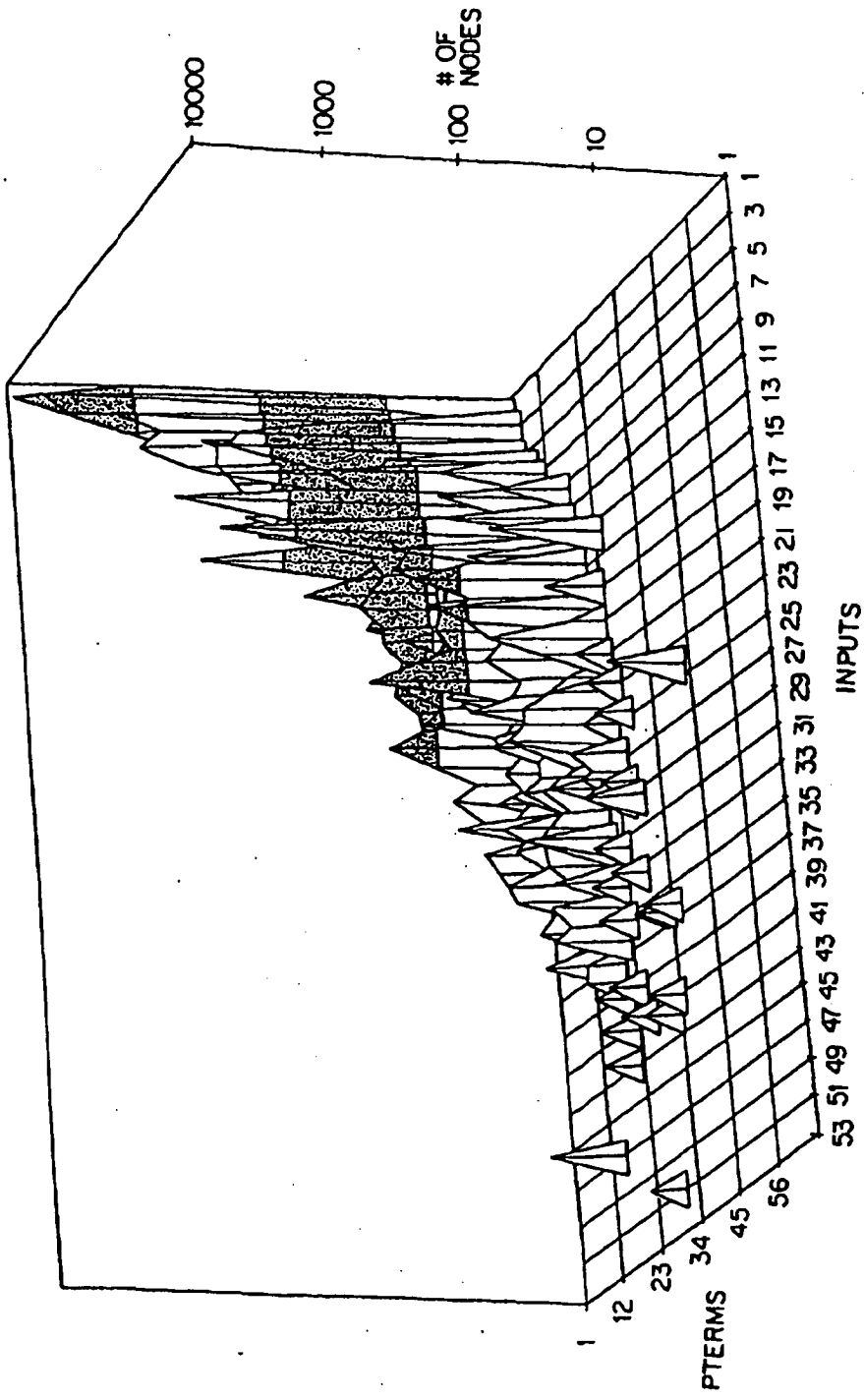
OF NODES
10000
1000
100
10
1
1 3 5 7 9 11 13 15 17 19 21 23 25 27 29 31 33 35 37 39 41 43 45 47 49 51 53
INPUTS
1 12 23 34 45 56
PTERMS

FIG. 7

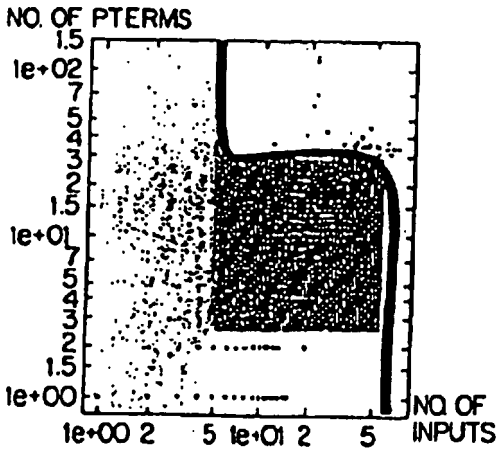

FIG. 8

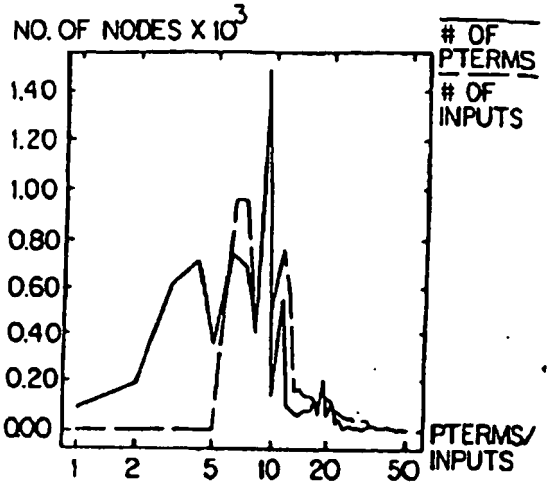

FIG. 9

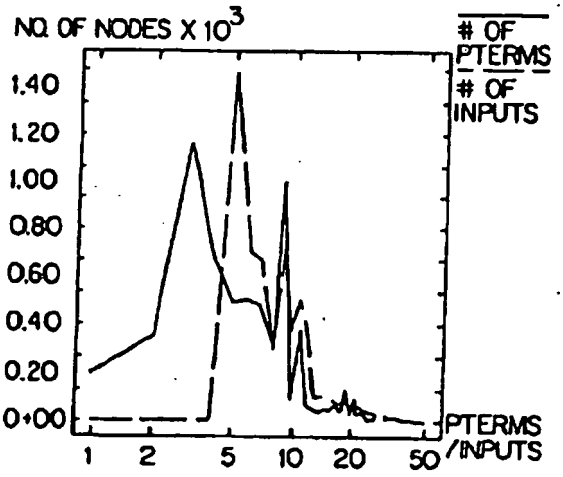

FIG. 10

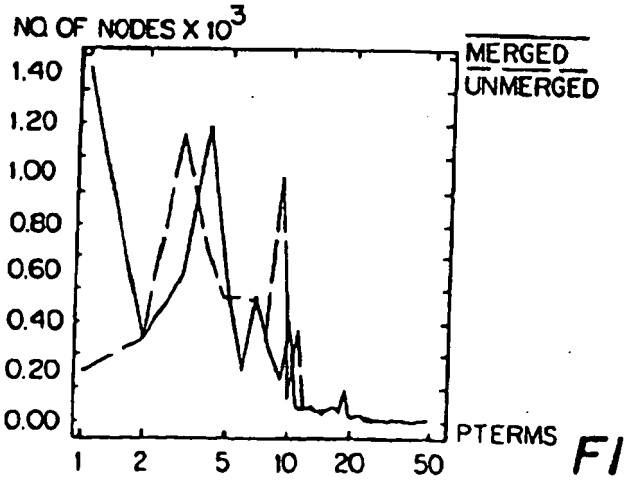

FIG. 11